

FIG. 1

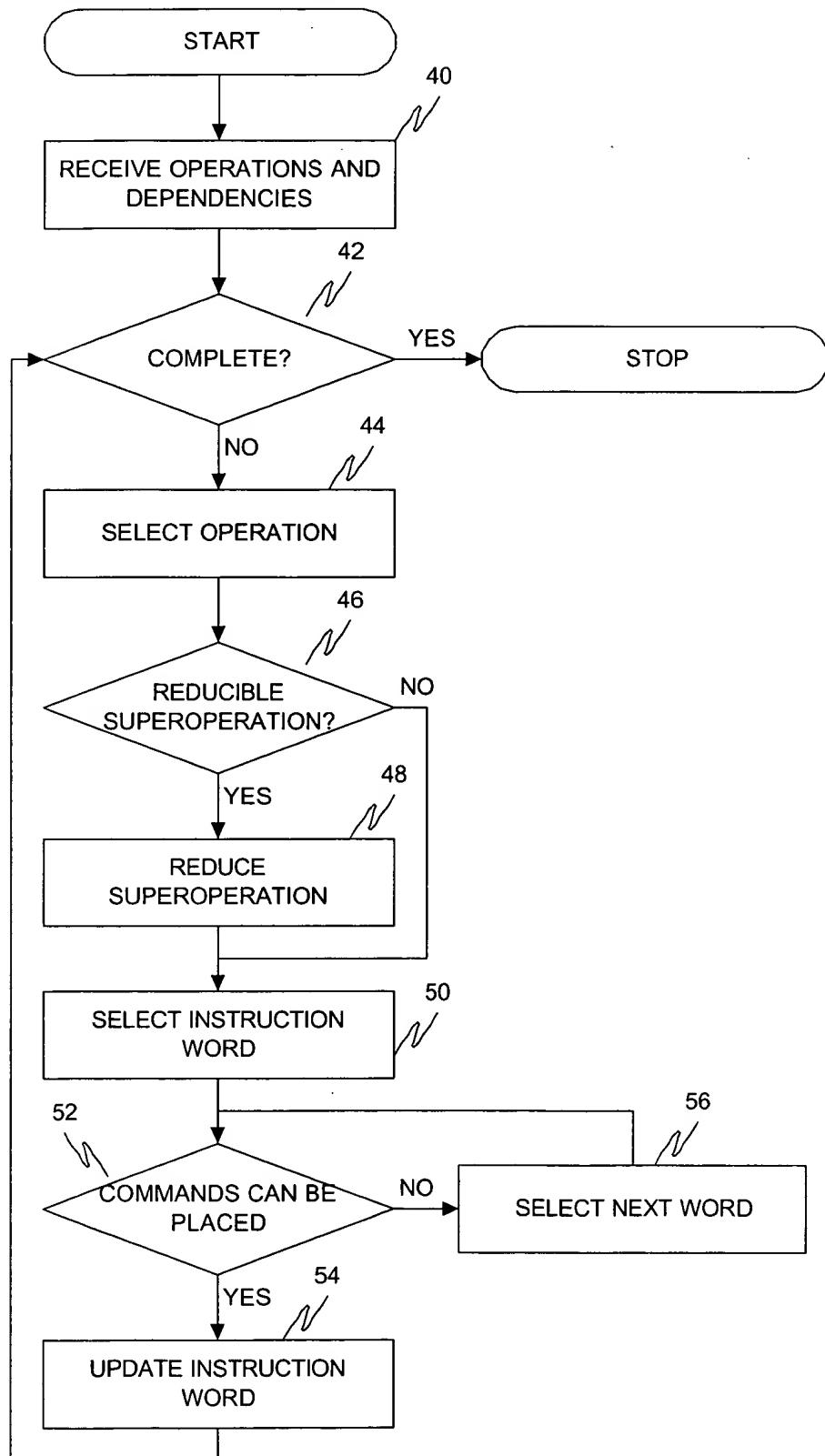


FIG. 2

Title: Combining Operations in a VLIW

processor

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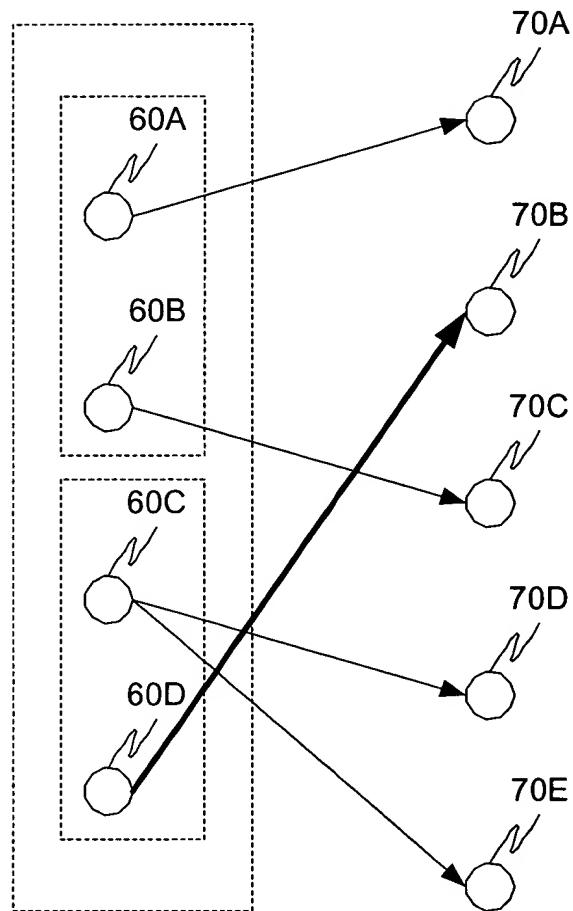


FIG. 3

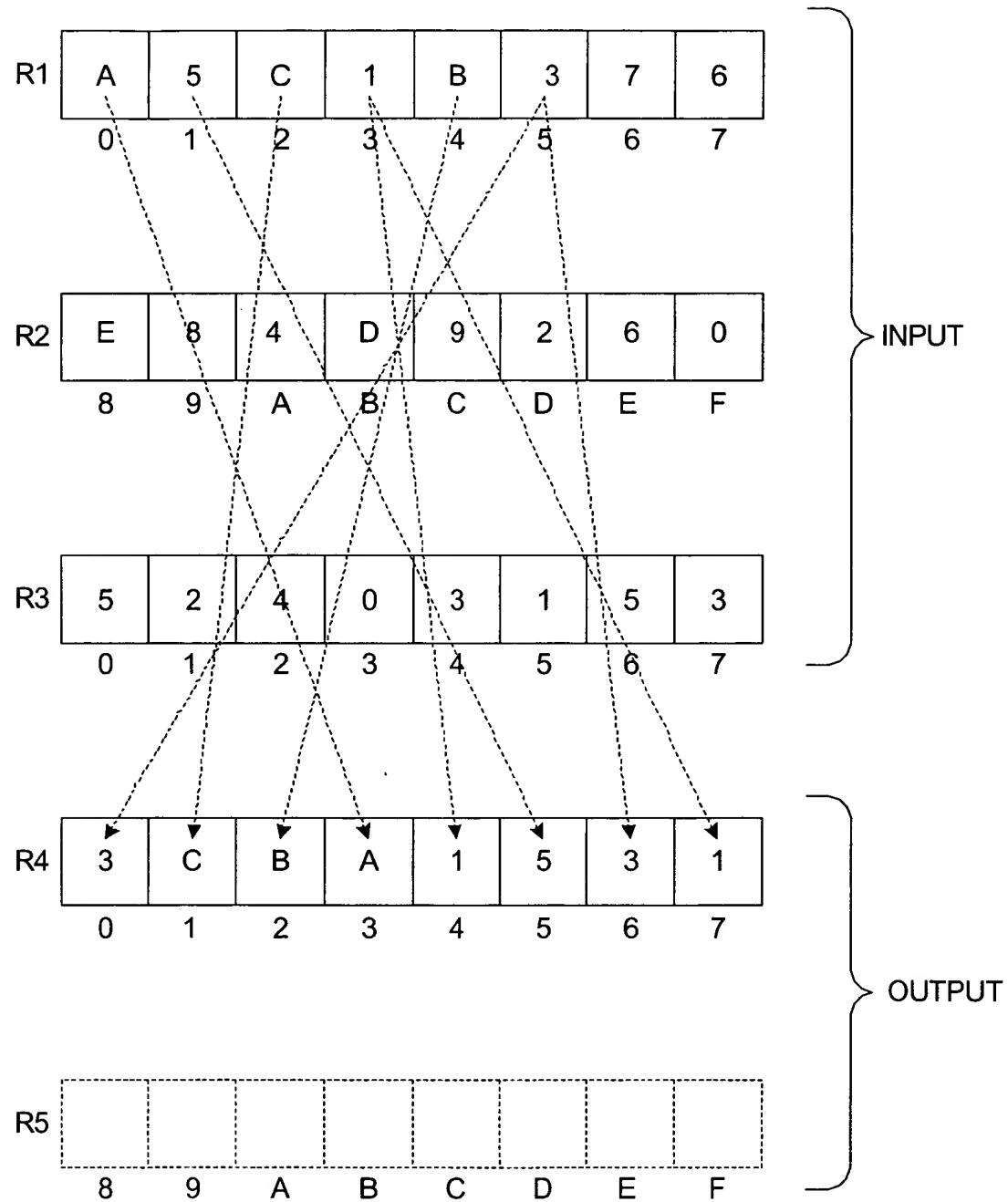


FIG. 4

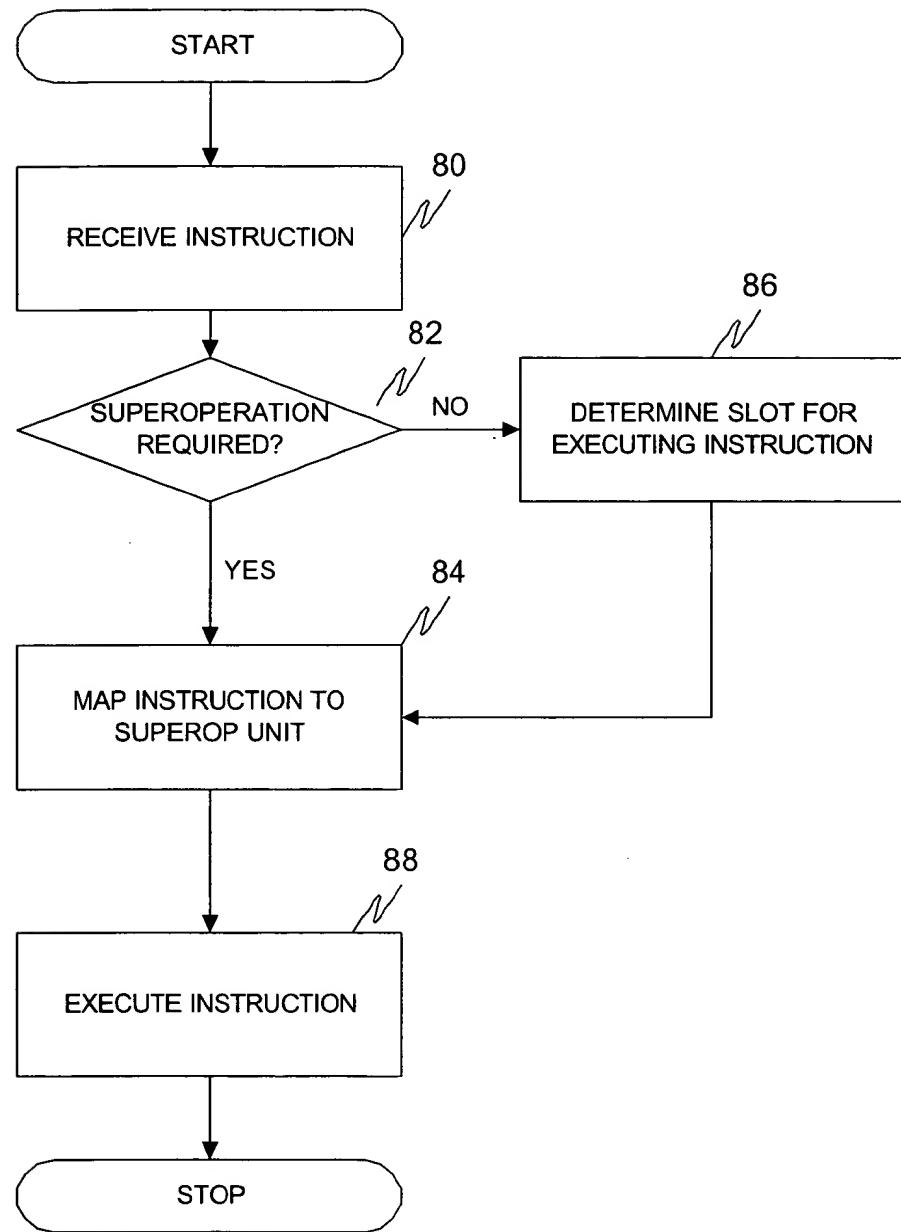


FIG. 5